Challenges in Tackling Reset Domain Crossing Verification with Low Power SoC

- Francis Chockalingam – Broadcom, Bangalore, India
- Viral Gorasia – Broadcom, Bangalore, India
- Anup Gupta – Synopsys, Bangalore, India
- Amit Goldie – Synopsys, Noida, India

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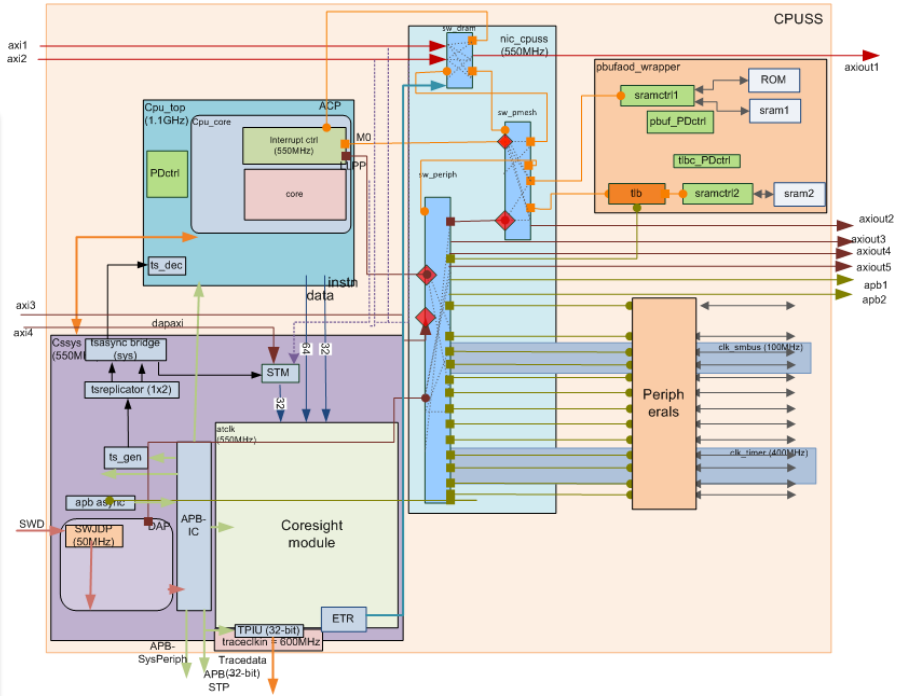
Design Details and Challenge

- Processor complex
  - AXI bus fabric, System ROM/Memory, TLBC, Peripherals
- Clocks
  - CPU: 1.1GHz, System: 550MHz,
  - Peripherals: 25/100/400/550MHz,
  - Debug: 10/40/550/595MHz
  - Design blocks operate in a range of frequency requiring multiple CDC-modes
- CPU complex consists of 5 power-islands
  - Clock gating in Standby/Snooze mode
  - Low-power modes for memories
  - Results in 48 low-power states
- Power up/down and power-mode transition sequence
  - Clock/Reset ordering
  - Retention state restored
  - Memory wakeup/sleep handshake

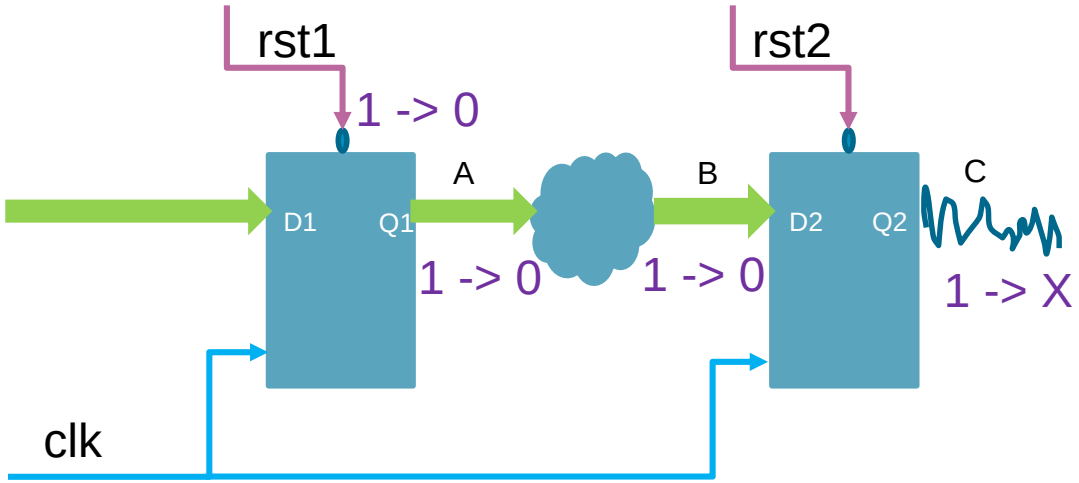


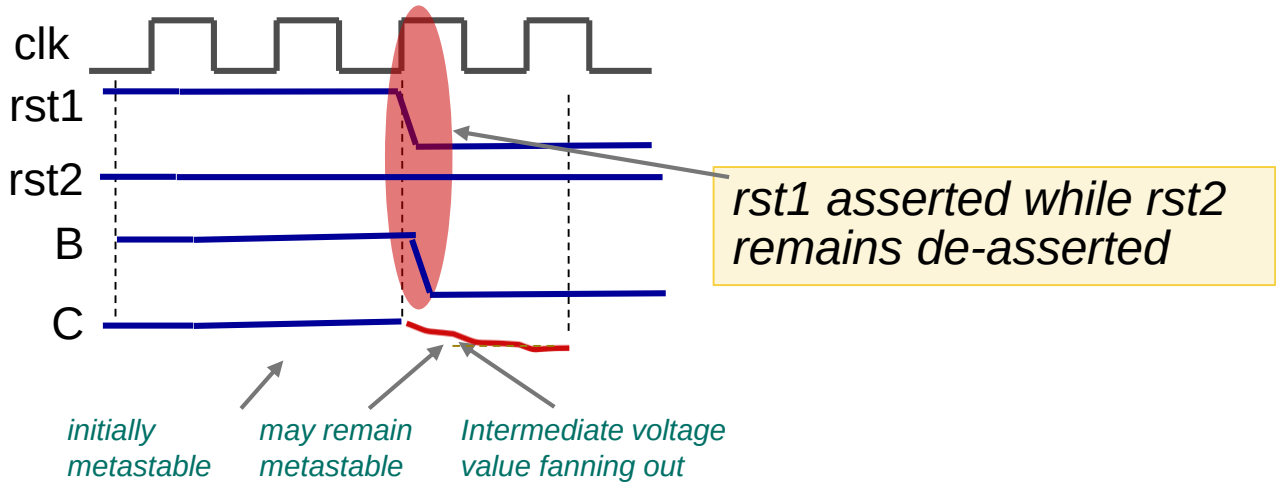
CPU	Single-core
Fabric	26 master 7 slave
Peripherals	13
Design Size	2M gates
Memory	1.2MBytes
Clock domains	11
Reset domains	27
Power domains	5
Power States	48

Verification of clock, reset and power domain crossing a challenge

Reset-domain crossing

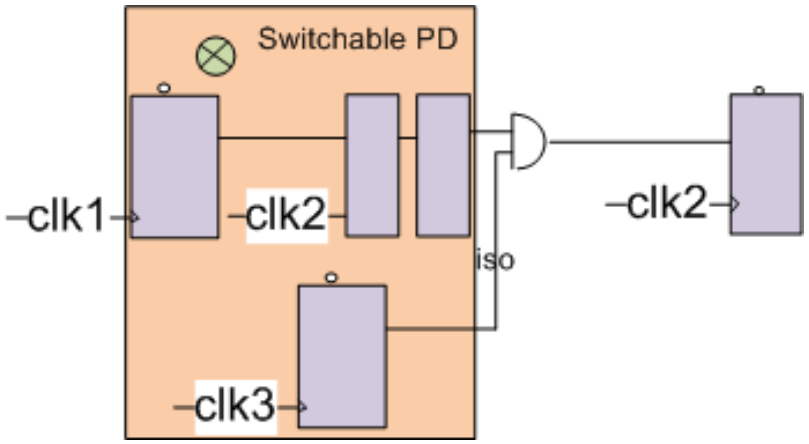
- Reset assertion places the sequential element in a defined state
- Resets are asserted asynchronously and de-asserted synchronously
- Asynchronous reset assertion means asynchronous flop output transition
- Particular reset assertion while the reset of a downstream flop remaining de-asserted causes reset-ordering issue
- Incorrect reset ordering even between flops of same clock domain
  - Causes setup/hold violation between reset and flop input at the destination
  - Results in a meta-stable condition in the destination flop



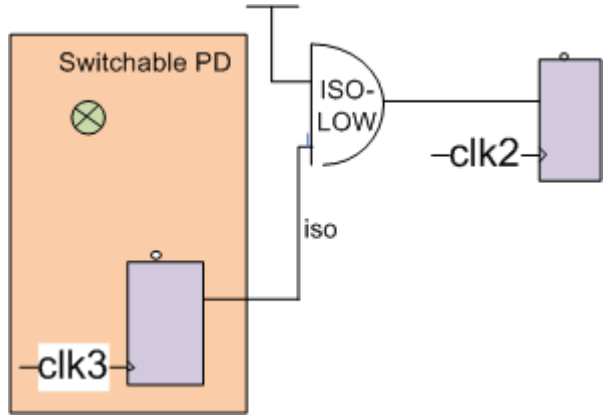


Power-domain Crossing

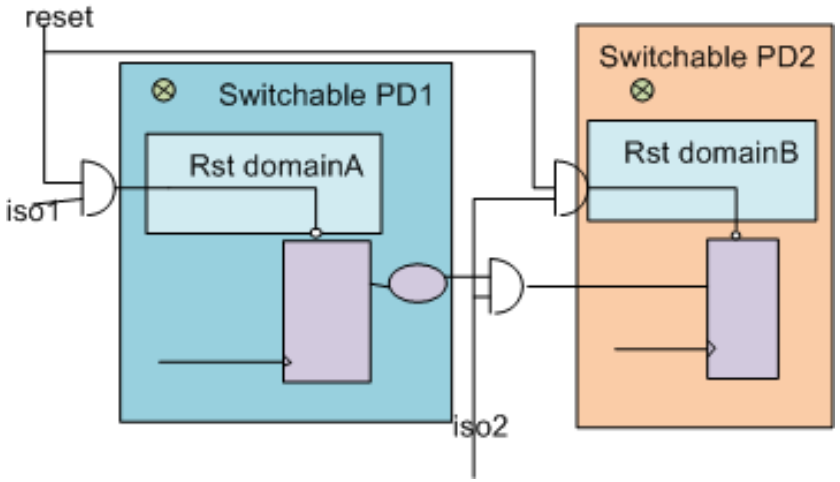
- SoCs require ever-increasing performance at the same or lesser power envelope
  - This is enabled using multiple power, clock and reset domains
- Power intent specification consists of power-domains, power-supply, isolation cells, retention logic and power states
- Power-state transition requires reset assertion and clock enabling
- Clock-enables in the power-up sequence needs to be proper



CDC metastability due to isolation



Metastability due to clamp value mismatch



Metastability due to RDC across PD

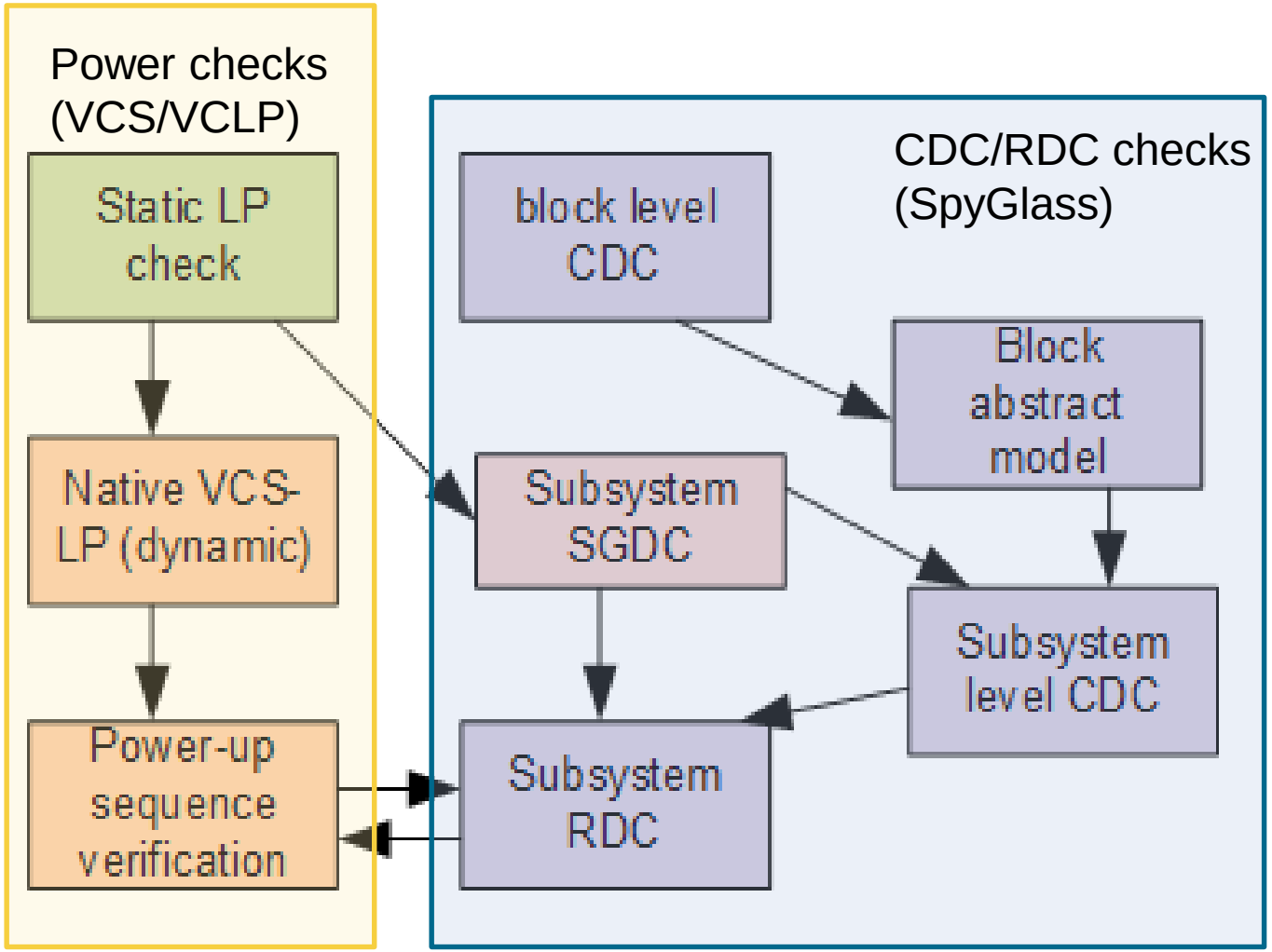
Challenge: RDC verification with multiple PDC

- Power up/down sequence and reset sequences are very inter-related
  - Reset required after power-up of the respective power-islands
  - Verifying reset-ordering requirements for the various power-gating scenario is challenging
- Static and dynamic UPF checks does not address the reset sequencing in PDC
  - RDC check needs to be done in the context of power-intent of the subsystem
  - Isolation de-assertion could result in reset-ordering during power-state transition
- RDC and UPF-aware static/dynamic verification setup needed to be enhanced
  - To address the reset-ordering requirement for the various power-states
  - To ensure retention states of the reset synchronizers are proper

Reset verification in the context of power-up sequence extremely critical to avoid silicon issues

Proposed Verification flow

- SpyGlass RDC uses the reset order constraints
  - UPF power-states and power-mgmt controller state transition are used to create the reset order constraints
  - Without reset order constraints, large no. of RDC violations are seen
- Reset order constraints using power-states
  - Power-states transition from VCS-NLP report parsed to identify reset-order (`define_reset_order`)
  - UPF Power-state coverage enhances the Power-mgmt controller stimulus
  - Helpful in addressing power-gating corner cases of reset ordering
  - Flags the reset-synchronizer retention state issues
- Reset constraints pruned using Power management controller FSM coverage
  - used to take out any invalid power-domain crossing
  - refine the illegal reset constraints which could create false RDC violations (`reset_filter_path`)



Traditional CDC/RDC checks integrated with LP checks for PDC verification

RDC violation pruning

- SpyGlass GuideWare methodology used with rdc_verify_struct for RDC check
- Initial RDC run gave around 16,200 Ar_resetcross01 violations
  - Run took around 40minutes when run at the RTL level (2M gates)
- Power up sequence reset order was obtained from parsing Pwr management controller stimulus
  - This was used to create the define_reset_order constraints
- Reset relationship between flops without reset were obtained using a primetime script.
  - This list was used to create reset_filter_path constraints
- Reset order constraints resolved ~15k
  - 1090 warnings remaining
  - They were due to Reset logic passing through the lesser-ON power-islands

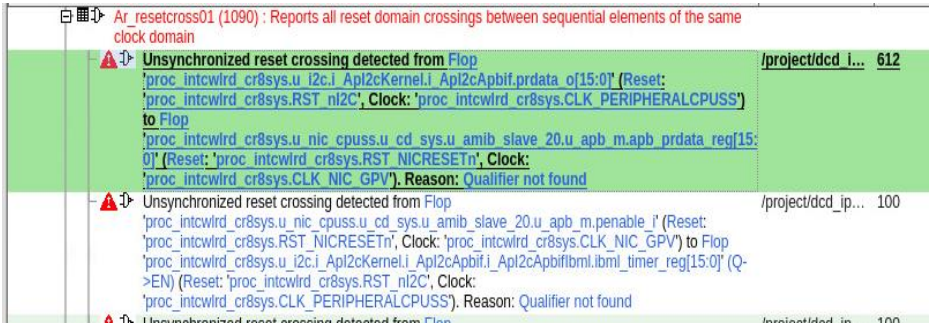
```
# cr8 scureset and periphreset asserted/deasserted together
define_reset_order -from RST_nSCURESET -to RST_nPERIPHRESETCR8

# Timer/pdctrl logic in AON domain which is isolated
# when powered-down
define_reset_order -from RST_NICRESETn -to RST_TIMERn[*]
define_reset_order -from RST_nCPURESET -to RST_nCPURESET_pdctrl
```

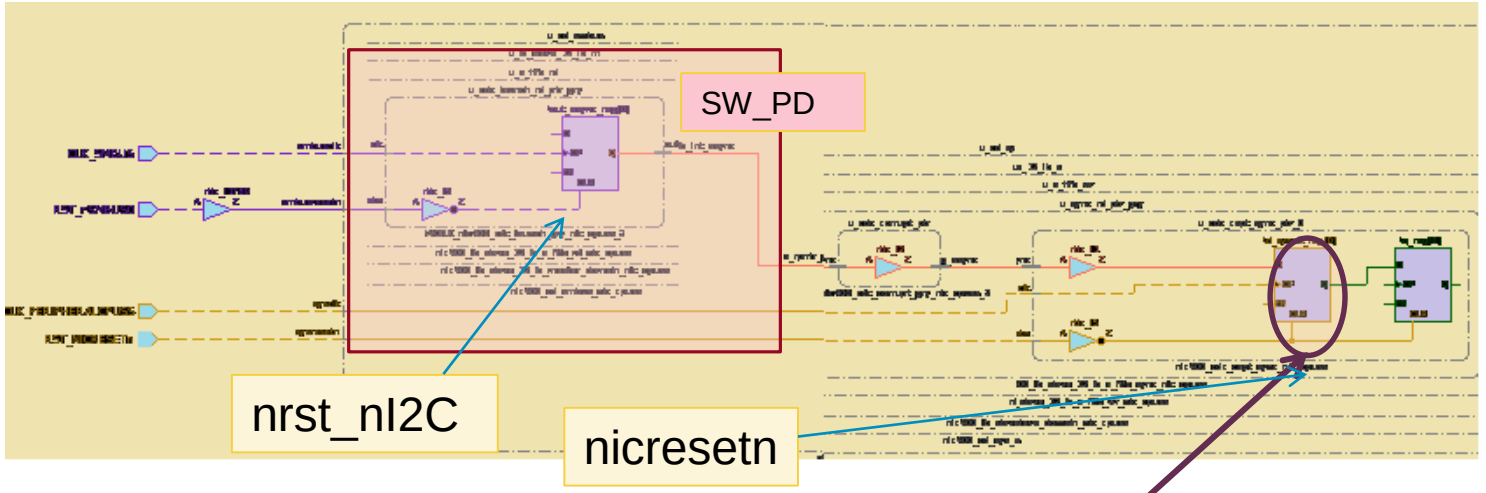
```
# periphreset to flops without reset
reset_filter_path -from_rst RST_nPERIPHRESETCR8 \
  -clock CLK_PERIPHERALCR8
reset_filter_path -from_rst RST_nSCURESET \
  -clock CLK_PERIPHERALCR8
```

RDC constraint setup streamlined using VCS/PT parser script

Issue #1: RDC issue due to PDC

- Remaining ~1K RDC violations were reviewed to be in the power-domain crossings
- SpyGlass GUI helped narrow down the issue to reset de-assertion from switchable domain
- Reset crossing from the switchable domain into more-ON power domains
  - Results in reset ordering issues during power up sequence
  - Fix was to introduce synchronizer cells in the receiving domain to avoid metastability



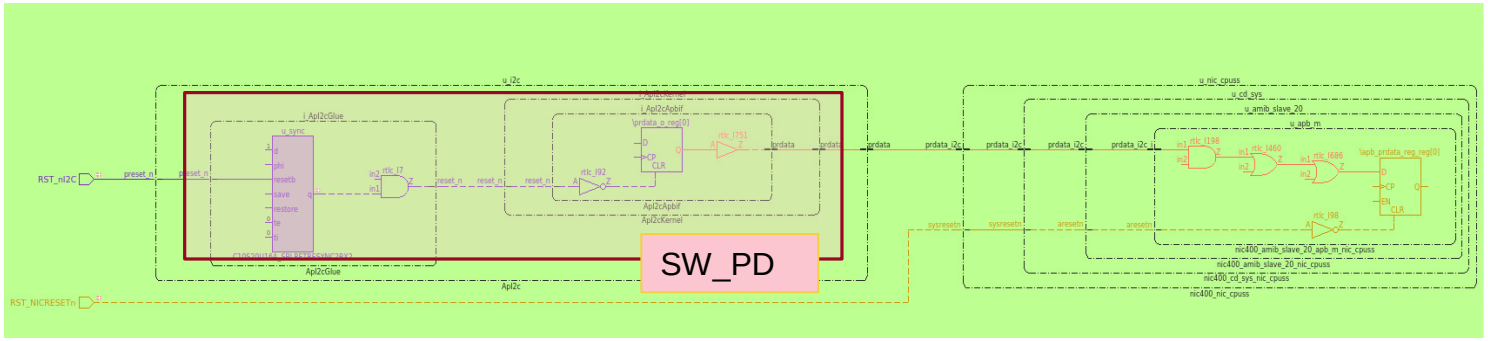



```
switchable domain with reset sync flops identified through VCLP parsing:
  - I2C(RST_nI2C, CLK_PERIPHERALCPUSS) -> PRDATA -> NIC (RST_NICRESETn, CLK_NIC_GPV)
  - NIC  (RST_NICRESETn, CLK_NIC_GPV) -> PENABLE -> I2C(RST_nI2C, CLK_PERIPHERALCPUSS)
  - SMBUS0(RST_nSMBUS0, CLK_SMBUS) -> PRDATA -> NIC (RST_NICRESETn, CLK_NIC_GPV)
  - NIC  (RST_NICRESETn, CLK_NIC_GPV) -> PENABLE -> SMBUS0(RST_nSMBUS0, CLK_SMBUS)
```

Metastability due to D->rstn

Issue #2: Power-island Reset synchronizer RDC

- Reset de-assertion with the reset synchronizer in the switchable domain flagged by SpyGlass
  - Clock is gated during power-down sequence, hence reset de-assertion is not propagated
  - Default state of sync-cell conflicts with isolation state
  - When clock is enabled after power-up cycle, there is a reset pulse causing RDC issue downstream
- One fix was to revise the power-up reset sequence to ensure clock being un-gated
  - This requires firmware update and verification of the reset sequence
- Other option was to use of retention reset synchronizer to retain the de-assertion value
  - No need to propagate the reset de-assertion as the de-asserted value will gets restored during power-up cycle
- PST messages from VCLP report were parsed to identify similar issue
  - Script refined to include this and revised reset constraints generated

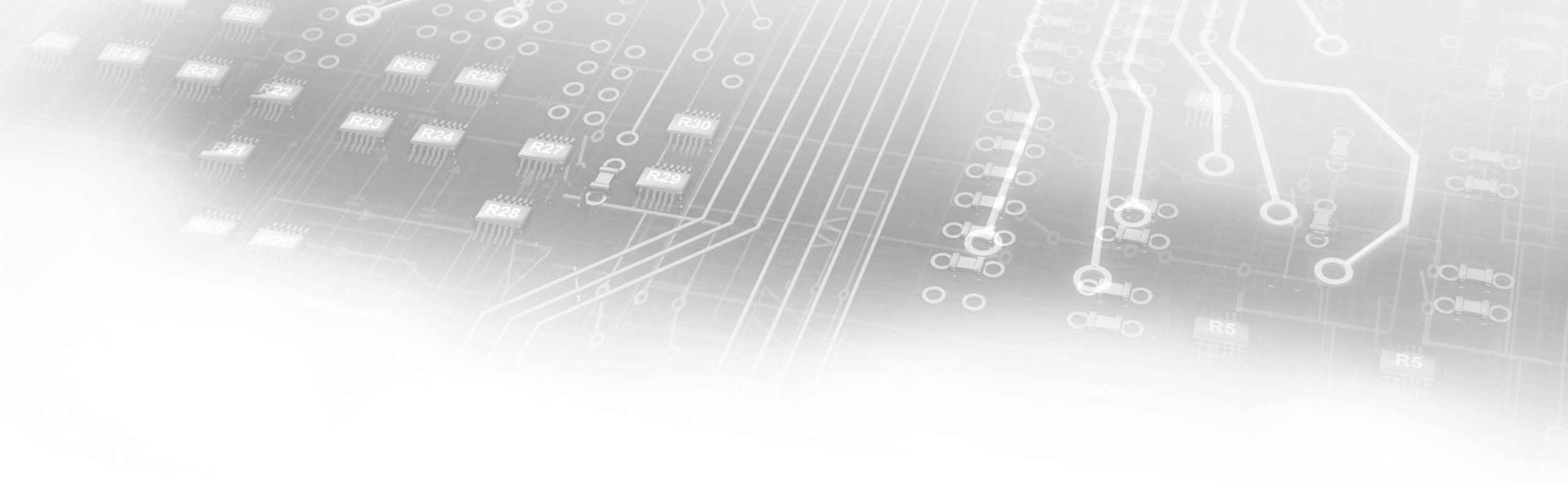


VCLP based reset constraints helped resolve the RDC violations

Results

- Enhanced verification flow aided in addressing the RDC violations flagged by SpyGlass
  - Large no. of RDC violations were pruned using define_reset_order and reset_filter_path constraints
  - Automated reset constraints generation using VCS/STA scripts reduced setup time from weeks to less than day
  - Script based constraint generation avoided any mistakes as well as made review easier
- Power domain related reset crossing issues Flagged with the proposed flow
  - Identified the Peripheral reset synchronizer retention requirement due to power-gating
  - Reset synchronizer retention states identified and updated UPF accordingly
  - Pwr-controller updated for proper reset sequence based on reset constraints
- Reset spec needs to be qualified with functional simulation and assertions
  - Reset ordering specification ensured a robust RDC
  - Functional simulation vectors were updated based on upf_state_machine.rpt
  - Reset assertion were defined based on intended sequence/ordering and coverage measured
- Updated reset constraints portable for both block and top-level RDC runs
  - Avoided time-consuming manual review of violations and waivers
- CDC/RDC checks were done at a very earlier stage of the project
  - Helped address the issues well in advance and not wait for timing-closed SDF simulation

Static and Dynamic checks come together for reset sequence signoff



Thank You

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